SESSION 14 – TAPA II
Analog Circuit Techniques

Friday, June 18, 1:30 p.m.
Chairpersons: T. Blalock, University of Virginia
K. Kotani, Tohoku University

14.1 — 1:30 p.m.
A Pixel-Parallel Image Processor for Gabor Filtering Based on Merged Analog/Digital Architecture, T. Morie, J. Umezawa* and A. Iwata*, Kyushu Institute of Technology, Kitakyushu, Japan, *A-R-Tec Corporation, Higashi-Hiroshima, Japan

Gabor filtering is a powerful feature extraction method for image recognition. We propose a pixel-parallel processor for Gabor filtering using a new algorithm with nearest-neighbor connections. The LSI has been designed using 0.35um CMOS based on the merged analog/digital architecture, which uses pulse-width modulation signals. The LSI includes 62x71 pixel circuits on a 9.8mm sq. chip area. Experiments using the fabricated LSI have verified that the spatial frequency of the image is correctly extracted.

14.2 — 1:55 p.m.
A Low-Power Switched-Current CDMA Matched Filter with On-Chip V-I and I-V Converters, T. Yamasaki, T. Nakayama and T. Shibata, The University of Tokyo, Tokyo, Japan

A low-power and compact CDMA matched filter has been developed using the switched-current technology. On-chip V-I and I-V converters featuring moderate linear characteristics have been developed for the chip. The low-power operation has been achieved by the sub-block architecture and the reduced current flowing in current-memory cells. A low-power clock-on-demand shift-register has also been developed. The 256-chip matched filter fabricated in a 0.35-um technology demonstrated 1.95mW operation at 8Mchip/s with 2V power supply, occupying 0.54mm2.

14.3 — 2:20 p.m.
An Area-Efficient, Integrated, Linear Regulator with Ultra-Fast Load Regulation, P. Hazucha, T. Karnik, B. Bloechel, C. Parsons, D. Finan and S. Borkar, Intel Laboratories, Hillsboro, OR

We demonstrate a fully-integrated linear regulator for multi-supply-voltage microprocessors implemented in a 90nm CMOS technology. Ultra-fast, single-stageload regulation achieves 0.54ns response time at 94% current efficiency. This enables 10% peak-to-peak output noise for a 100mA load step with only a small on-chip decoupling capacitor of 0.6nF. A PMOS pull-up transistor in the output stage results in a small regulator area of 0.008mm2 and the 0.6nF MOS capacitor area of 0.090mm2.

14.4 — 2:45 p.m.
A Circuit Design-Based Approach for 1/f-Noise Reduction in Linear Analog CMOS IC's, J. Koh, R. Thewes, D. Schmitt-Landsiedel* and R. Brederlow, Infineon Technologies AG, Munich, Germany, *Technical University of Munich, Munich, Germany

A new circuit design based approach for 1/f noise reduction in linear analog CMOS circuits is presented using a device physics based effect. Compared to a reference circuit, a threefold reduction (5 dB) at 10Hz in 1/f noise is achieved for an operational amplifier designed in a standard 0.12µm, 1.5V CMOS technology.

Break 3:10 p.m.